Amendments to the Specification

Please amend the last paragraph on page 1 of the specification as follows:

To this end, various solutions are known which deal with a respective advantageous variant for the synthesis of a VLIW (~~very~~ Very Long Instruction Word) from the instruction words which arise during the program cycle.

Please amend the fourth paragraph on page 5 of the specification as follows:

In one variant, the inventive object is achieved by implementing a "Command Code" mode of operation of the HVLIW and its associated general header. The Command Code mode of operation may be similar to the mode commonly known as VLIW mode. This general header stores the information, in coded form, which indicates all combinations regarding which first and second FIW (instruction word part) is provided, after decoding, in the execution phase, for actuating a respective first and/or second FU (function unit) in the processor.

Please amend the penultimate paragraph on page 5 of the specification (preceding the last sentence "This saves memory space and conserves processor performance" on the page) as follows:

The aim of this solution is for the desired compression of the instructions to be implemented in the "Command Code" mode of operation of the HVLIW by combining [[a]] plurality of FIWs and an associated combination of the details regarding which of the FUs is to be actuated by which FIW, and also which FIW takes up particular memory locations in the cache when the VLIW is constructed and which operations are then executed with the memory content of said memory locations in relation to other memory locations in the cache.

Please amend the fourth paragraph on page 5 of the specification as follows:

In one variant, the inventive object is achieved by implementing a "Command Code" mode of operation of the HVLIW and its associated general header. The Command Code mode of operation may be similar to the mode commonly known as VLIW mode. This general header stores the information, in coded form, which indicates all combinations regarding which first and second FIW (instruction word part) is provided, after decoding, in the execution phase, for actuating a respective first and/or second FU (function unit) in the processor.

Please amend the penultimate paragraph on page 6 of the specification as follows:

This inventive solution lays emphasis on "Command Mode" mode of operation with general header which is very flexible and types of "Command Code". This ~~is also providing the a~~ also provides structured supports all intended to remain valid for further development and updates and to safeguard its compression options.

Please amend the last paragraph on page 6 of the specification as follows:

A further variant of the inventive manner of achieving the object is for a "reference instruction" mode of operation of the general header to be implemented in which the FIWs provided for constructing the VLIW in the execution phase are buffer-stored generally in the cache. The reference instruction mode referred to herein may be similar to the operation mode SIMD in the art.

Please replace the paragraph bridging pages 10 and 11 of the specification with the following paragraph:

The following is a list of the reference numerals used in Figures 1 and 2:

1. TVLIW (Tagged Very Long Instruction Word)
2. First operating code
3. First tag
4. First FIW (Function Instruction Word part)
5. Second operating code
6. Second tag
7. Second FIW
8. Code analyzer
9. Dictionary
10. HVLIW (Headed Very Long Instruction Word)
11. First TVLIW container
12. Second TVLIW container
13. General header
14. Header mode

15. FU-C information (Function Unit Combination information)

16. CE information (cache Extra information)

17. Supplementary information

18. Code converter

19. First FU (Function Unit)

20. Second FU (Function Unit)

21. Processor

22. VLIW (Very Long Instruction Word)

23. Decoder

24. Header decoder

25. CMDT (Command Code Decompression Table)

26. Cache

27. Cache miss repair logic unit

Please amend the second paragraph on page 12 of the specification as follows:

As can be seen in Figure 1, in the configuration phase the starting point for the inventive compression is the presence of the TVLIW 1. In an exemplary embodiment this comprises the first and second TVLIW containers ~~11; 12~~. 11, 12.